# A flex architecture for systems with embedded, spatially-distributed sensors

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## Introduction

There is an important new class of systems that are best served by an architecture that is the opposite of system-on-a-chip. Really small chips that integrate accurate sensors and A/D conversion elements have become a very effective means of implementing embedded spatially-distributed sensors. A reconfigurable computing element can efficiently interface a number of such sensors to produce a system with compelling economic and performance advantages. We propose a novel architecture for this class of systems. We report the design of three chips that can use this architecture to good advantage.

- Chip #1 is a precise temperature sensor with integral heating capability.
- Chip #2 is a microphone-to-bits signal processing circuit.
- Chip #3 is the PDSP (parametric digital signal processor), a reconfigurable computing element.

Chips 1 and 2 each have 6 pads and their sizes (just active area) are 150 and 600 microns square, respectively. These mostly-analog chips have been designed in 0.6 and 0.35 micron technologies, respectively. For practical reasons, prototype Silicon uses conventional packaging and diesize is completely dominated by pads and ESD structures. Only in very recent times has it become possible to physically handle and package such small chips efficiently. At ISSCC03, Hitachi reported an RFID chip of diesize 330 microns square [1]. Alien Technologies has developed fluidic self-assembly techniques for handling even smaller chips [2].

. For development purposes, we have built chip #3 as an FPGA. Estimated diesize in 0.18 micron technology is less than 300 microns square.

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## Architecture

One novel aspect of this architecture is the way we split up the A/D conversion.

Conventional approaches:

1. Take a strictly analog output from the sensor chip to the data converter, which often is integrated as a system-on-a-chip.

2. Put a sigma-delta converter right in the sensor, along with an inflexible, hard-wired block of logic that locally filters and decimates to generate a digital output from the sensor chip to the processor.

Our approach (figure 1)

Integrate the analog portion of the sigma-delta on each of numerous sensor chips, which send out an oversampled data streams. The PDSP then filters and decimates these data streams. Optionally, the PDSP provides feedback to the sensor chips in order to implement adaptive sense or control algorithms.

The PDSP

We have developed a parametric digital signal processing block that does the filtering and decimation at an especially low power level. In conventional systems, these functions are performed with hard-wired logic rather than with a conventional DSP, in order to save power. Our PDSP block serves as a satellite DSP, and achieves even lower power levels than the hard-wired alternative. Typically the PDSP occupies only a very small fraction of the area of the processor chip.

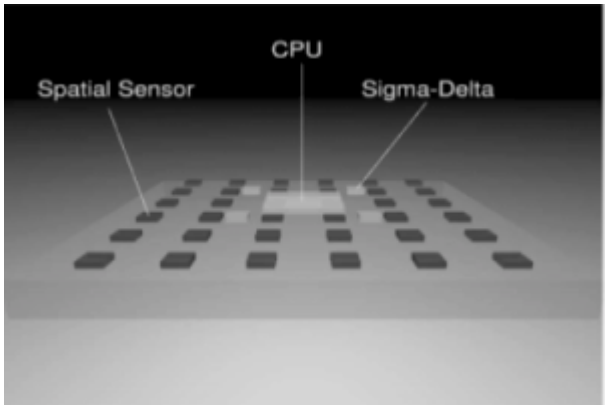

Figure 1

## Implementation of the architecture

From an electronic point of view, we are considering systems that are built with the following types of chips:

- Sensor, with on-chip analog signal processing chain
- Digital processing element

This approach is the opposite of 'system-on-a-chip'. The necessity of spatially distributing the sensor clearly drives the partition. The partition brings a lot of additional benefits:

- Dynamic range gets better because substrate noise coupling is eliminated.
- Power is generally reduced, since the processor chip is typically built with a smaller-lithography process.
- Phase delay ceases to be a 'hard limit', since the processor DSP can dynamically alter the phase-delay-vs-power tradeoff.

## Flex Issues

Systems with embedded, spatially-distributed sensors impose the following requirements on the flex:

- Spatial distribution
- Very small chip size
- Increased vulnerability to ESD during manufacture
- Intolerance to noise and cross-coupling
- High-bandwidth, power-efficient transmission lines
- Flexibility

## Application: OCXO (Oven-Controlled Crystal Oscillator)

Flex technology with very small embedded chips is likely to improve OCXO performance sufficiently to allow OCXO's to be used in economically important applications that currently require atomic clocks.

The OCXO is one example of a system that contains embedded, spatially-distributed sensors. In this case, the sensors are typically thermistors that monitor, with

precision on the order of $10^{-3}$ Kelvin, the temperature distribution. A local processor then feeds back control information to embedded heating elements, in order to achieve good thermal regulation at the “turnaround temperature”, where the crystal’s TC goes through an inflection point.

Figure 2 shows the active area of a sense chip optimized for this application. Physical size, including the on-chip analog support electronics, is less than two hundred microns square. This is too small for conventional interconnect.

We have designed a thermal sense element and on-chip processing circuitry. It is based on a conventional Widlar pair of bipolar transistors, whose base-emitter voltages differ by kT/q times the natural log of the difference in the current densities at which we choose to operate them. With a little optimization we find that we can achieve a noise floor on the order of ten microdegrees Kelvin, assuming that the sensor is placed within a suitable sigma-delta conversion loop.

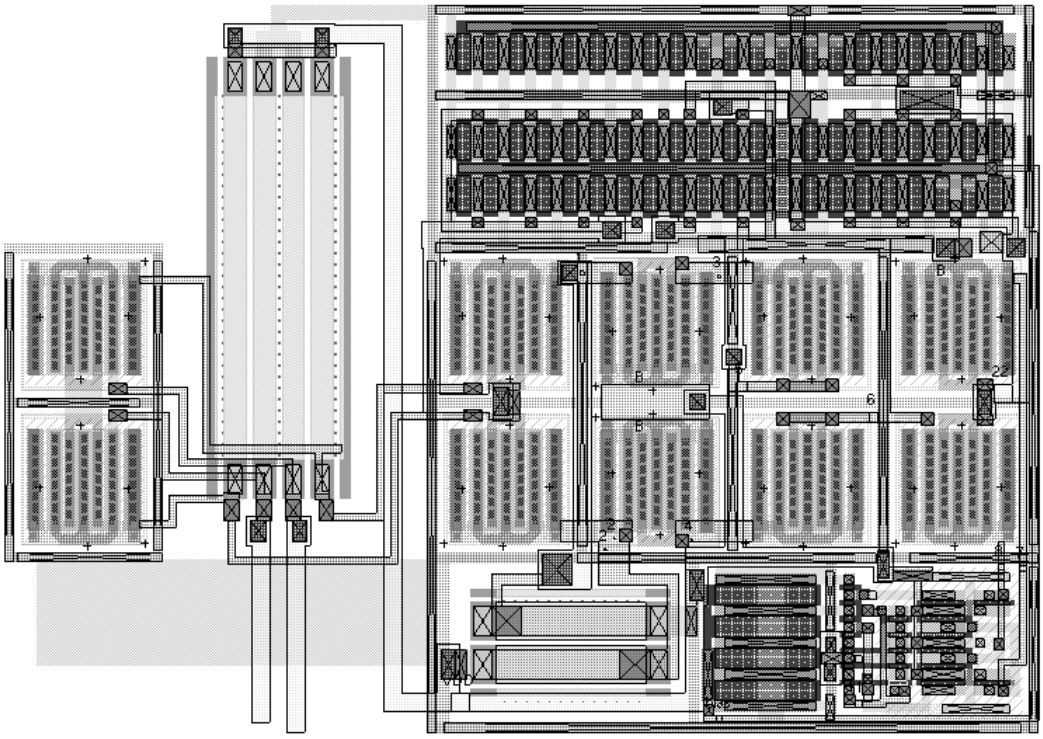

Figure 2

## Application: Inflammation sensor, for vascular imaging probe

On an experimental basis, ultrasound probes are used for imaging of vascular walls. Typically, a probe whose diameter is about 3 mm, is attached to a catheter that is pushed into the patient's artery for a distance of many centimeters. The flex that contains the probe also typically contains a temperature sensor that proves quite useful in the diagnosis of inflammation [3]. The temperature sensor would be yet more useful if it could sense spatial temperature variations as well.

As far as the temperature sensor is concerned, this is essentially the same application as the OCXO.

## Application: VOIP cellphone

Consider the cellphone. This system always has at least one embedded sensor (the microphone). Sometimes two or more microphones are used in order to cancel of background noise or provide spatial diversity.

To explain Intel's view of the rapid evolution of the human-to-cellphone interface, Jay Heeb introduced the notion of a *biogasket* [4]. The brain sits on one side of the biogasket and the cellphone's processor sits on the other side.

In the Tx direction, speech is the communication modality of greatest bandwidth and utility. This is where our present work is focused.

In the Rx direction, vision wins. High on Heeb's wish-list is video (preferably holographic) projection. Given the rapid advances in lasers and grating-valve technology, this far-fetched concept may not be so impossibly distant as it sounds. But it is certainly beyond the scope of this paper.

With the advent of the VOIP cellphone, there is strong incentive for improvement of the performance of embedded microphones. μ-law telephony compromises the quality of audio signals to an extent that is painfully obvious to the human ear. Less obvious but perhaps more important is the extent to which these quality issues compromise the performance of speech recognition.

Another related development is the MEMs microphone, which can be completely on-chip. Noise considerations of these devices make it particularly desirable to integrate an array of them on the flex.

Figure 3 shows the active of a chip we built in 0.35u CMOS to address this application. It is designed to be embedded within an electret microphone, in lieu of the FET that is customarily used to provide the first level of amplification. Because the output of this chip is a digital stream, it is almost completely insensitive to RFI.

Active area of this chip is about 400 microns square, in 0.35u CMOS.

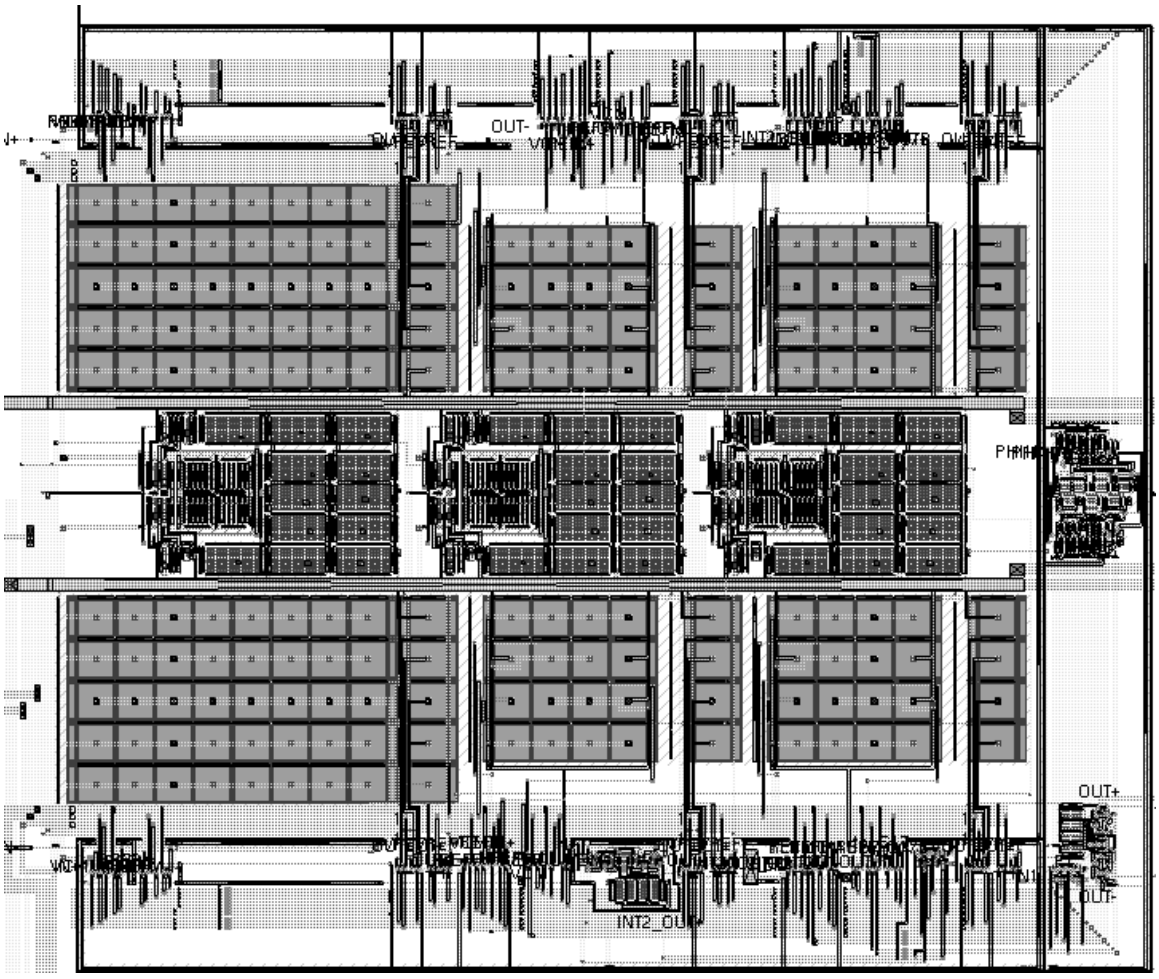


Figure 3

References:

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[3] B. Courtney, “Advances in Vascular Tissue Characterization and Imaging” IEEE EMBS Speech given 16 October 2002 at Stanford Medical School

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